**The Fetch-Execute Cycle**

Sort the following phrases into the correct sequence for the fetch-execute cycle:

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| **Fetch phase** | |
| * The address of the next instruction is held in the Program Counter | |
| * The address is copied from the Program Counter to the Memory Address Register | |
| * The instruction stored at that address is copied to the Memory Buffer Register | * At the same time, the contents of the Program Counter are incremented by 1, ready for the next instruction |
| * The instruction is copied to the Current Instruction Register | |
| **Execute phase** | |
| * The instruction held in the Current Instruction Register is decoded | |
| * The instruction is executed | |

**Challenge: Examples of the Execute phase**

Sort the following phrases into the correct sequence for the execute phase of a LOAD operation, ADD operation and STORE operation:

For LOAD operation (e.g. LDA 106):

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| * The operand part of the instruction is copied to the Memory Address Register |
| * The contents of that memory address are copied to the Memory Buffer Register |
| * Contents of the Memory Buffer Register are copied to the Accumulator |

For ADD CONTENTS OF MEMORY LOCATION operation (e.g. ADD 107):

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| * The operand part of the instruction is copied to the Memory Address Register |
| * The contents of that memory address are copied to the Memory Buffer Register |
| * Contents of the Memory Buffer Register are added to the value held in the Accumulator |

For STORE operation (e.g. STO 108):

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| * The operand part of the instruction is copied to the Memory Address Register |
| * The contents of the Accumulator are copied to the Memory Buffer Register |
| * Contents of the Memory Buffer Register are copied to the address held in the Memory Address Register |